CLAIM AMENDMENTS

The following is a complete list of claims. The claims below replace all prior versions of the claims in the application. Please amend claims 1, 13, 18, 20, 21 and 22.

1. (Currently Amended) An integrated circuit assembly comprising:

   a die ~~substrate~~ of semiconductor material including a circuit disposed in the die; ~~integrally formed therein;~~

   an interconnection layer for carrying a signal, ~~to and from a portion of the circuit,~~ the interconnection layer overlying the die ~~substrate~~ and making selective electrical connection to the circuit, ~~integrally formed in the substrate,~~ the interconnection layer formed of a first conductive material; and

   a distribution layer overlying the interconnection layer, the distribution layer including wire bonding pads for wire bonding to selected electrical signals, and distribution grids for distributing a signal over a region of the interconnection layer, the distribution grids connected to the wire bonding pads and extending over the interconnection layer, wherein at least one of the grids overlies the circuit and all of the grids together substantially cover the die, the distribution layer being formed of a second conductive material different from the first conductive material; and

   a plurality of connecting channels connecting selected ones of the distribution grids to selected locations of the interconnection layer.

2. (Original) The assembly of claim 1 wherein the first conductive material is copper.

3. (Original) The assembly of claim 2 wherein the second conductive material is aluminum.

4. (Original) The assembly of claim 1 wherein the second conductive material is aluminum.

5. (Original) The assembly of claim 1 wherein the connecting channels are vias.

6. (Original) The assembly of claim 1 wherein the selected locations of the interconnection layer include power connections and wherein at least one of the wire bonding pads is coupled to the power connections.

7. (Original) The assembly of claim 1 wherein the selected locations of the interconnection layer include ground connections and wherein at least one of the wire bonding pads is coupled to the ground connections.

8. (Original) The assembly of claim 1 wherein the connecting channels are distributed throughout the distribution layer.

9. (Original) The assembly of claim 1 further including a package having a surface including wire bonding pads, wherein the substrate is mounted on the package surface, and wherein the assembly further includes wire bonds coupling wire bonding pads of the package to the wire bonding pads of the distribution layer.

10. (Original) The assembly of claim 9 wherein the wire bonding pads of the package include ground and power pads.

11. (Original) The assembly of claim 1 wherein the wire bonding pads are disposed at the periphery of the distribution layer.

12. (Original) The assembly of claim 1 wherein the distribution grids form one of a star pattern and an orthogonal grid pattern.

13. (Currently Amended) An integrated circuit comprising:

a die ~~substrate~~ of semiconductor material having a circuit that includes a plurality of first supply nodes and a plurality of second supply nodes;

a first metalization layer overlying the die ~~substrate~~ and operable to couple a signal to multiple supply nodes of the circuit, ~~carry a signal~~ the first metalization layer including a first section connected to at least one of the first supply nodes and a second section connected to at least one of the second supply nodes, ~~to and from a portion of the circuit and~~ the first metalization layer formed of a first metal;

an insulator layer overlying the first metalization layer and including a plurality of vias; and

a second metalization layer overlying the insulator layer and making selective contact with the first metalization layer through the vias, the second metalization layer including a first region connected to the first section of the first metallization layer, and a second region connected to the second section of the first metallization layer, the first and second regions each operable to distribute a signal to multiple supply nodes, wherein at least one of the first and second regions overlies the circuit, and the first and second regions together substantially cover the die, ~~wire bonding pads and distribution grids coupled to the bonding pads and distributed over the insulator layer, each distribution grid operable to distribute a signal over a region of the first metallization layer,~~ the second metalization layer formed of a second metal different from the first metal.

14. (Original) The integrated circuit of claim 13 wherein the first metalization layer is formed of copper.

15. (Original) The integrated circuit of claim 14 wherein the second metalization layer is formed of aluminum.

16. (Original) The integrated circuit of claim 13 wherein the second metalization layer is formed of aluminum.

17. (Original) The integrated circuit of claim 13 wherein the vias are distributed throughout the insulator layer.

18. (Currently Amended) The integrated circuit of claim 13 further including a package having a surface including wire bonding pads, wherein the substrate is mounted on the package surface, and wherein the assembly further includes wire bonds coupling wire bonding pads of the package to wire ~~the wire~~ bonding pads of the second metalization layer.

19. (Original) The integrated circuit of claim 18 wherein the wire bonding pads of the package include ground and power pads.

20. (Currently Amended) The integrated circuit of claim 13 wherein the second metallization layer includes ~~the~~ wire bonding pads ~~are~~ disposed at the periphery of the second metalization layer.

21. (Currently Amended) The integrated circuit of claim 13 wherein the first region ~~distribution grids~~ forms one of a star pattern and an orthogonal grid pattern.

22. (Currently Amended) An integrated circuit comprising:

a die ~~substrate~~ of semiconductor material having a circuit disposed in the die;

a copper interconnection layer for carrying a signal, ~~to and from a portion of the circuit,~~ the layer overlying the die; ~~substrate and;~~

an insulator layer overlying the copper interconnection layer and including a plurality of vias;

an aluminum distribution layer overlying the insulator layer and making selective contact with the copper interconnection layer through the vias, the aluminum distribution layer including wire bonding pads and distribution grids for distributing a signal over a region of the interconnection layer, the distribution grids coupled to the bonding pads and distributed over the insulator layer, wherein at least one of the grids overlies the circuit and all of the grids together substantially cover the die; and

a package supporting the substrate and including ground and power bonding pads wire bonded to the wire bonding pads.